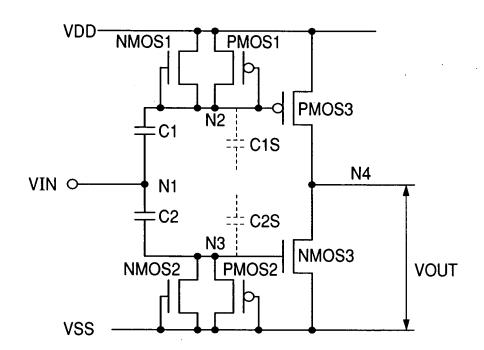
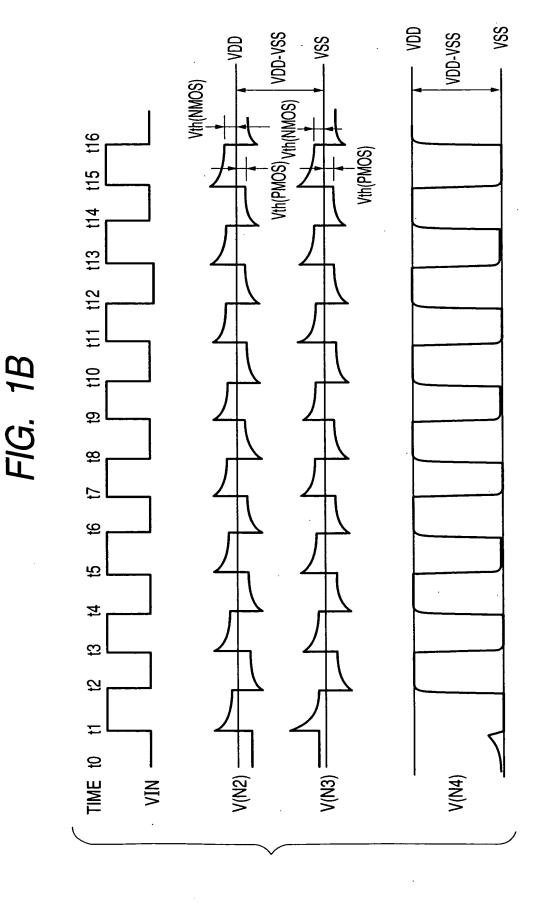
FIG. 1A





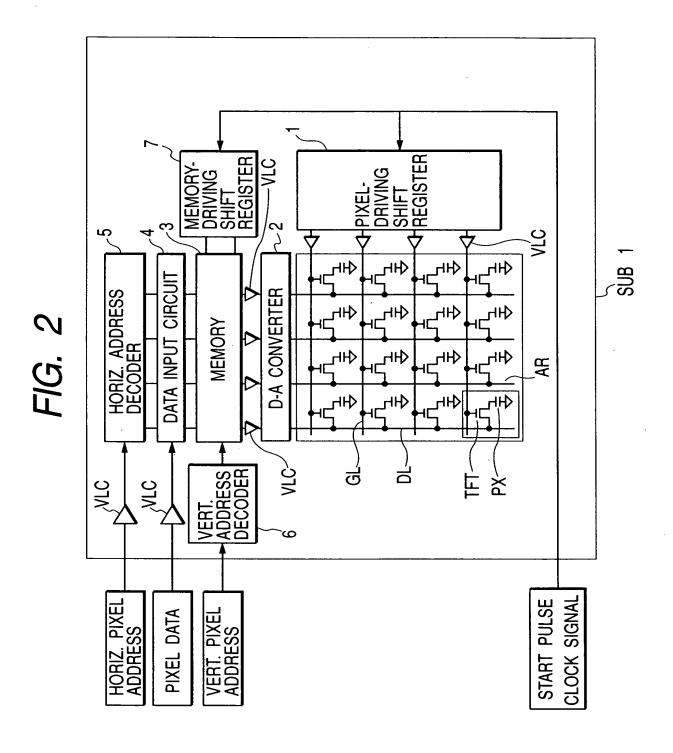


FIG. 3

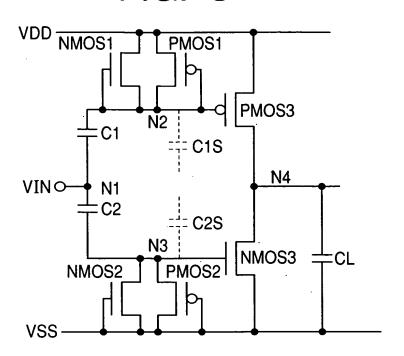
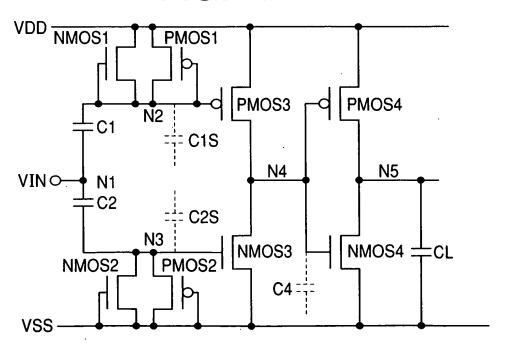
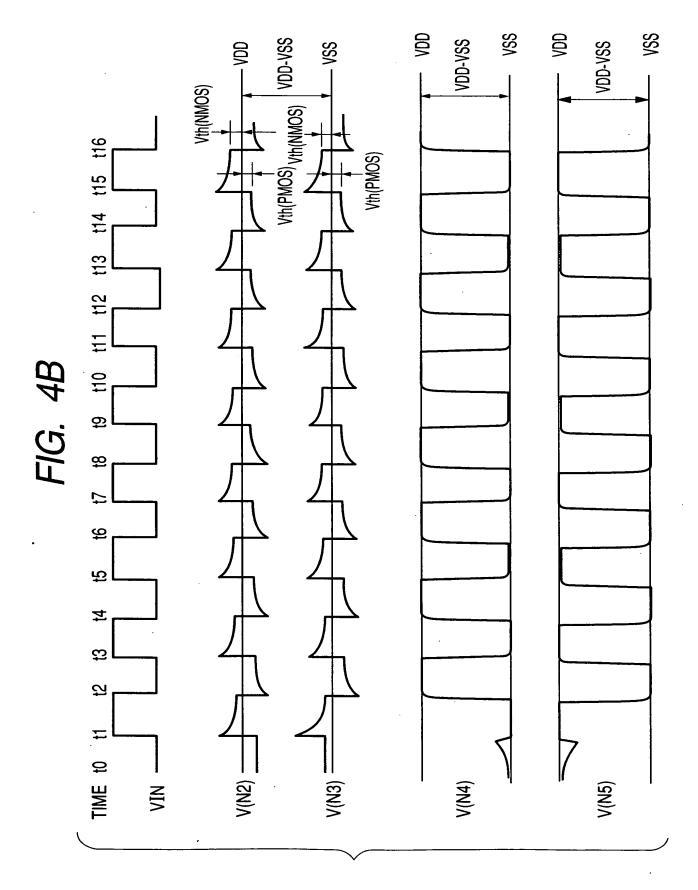


FIG. 4A





6/21 FIG. 5

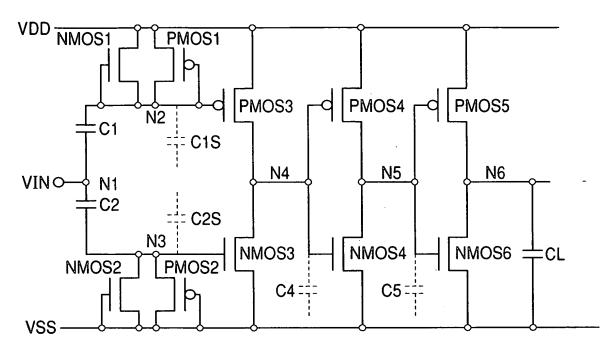


FIG. 6 VDD NMOS1 PMOS1 PMOS4 PMOS5 PMOS3 -d PMOS6 C1 === C1S N4 N5 N6 N7 VINO-ሳ N1 C2 =≟= C2S NMOS4 NMOS5 NMOS3 NMOS2 C4 = == C5=== C6 = == VSS-

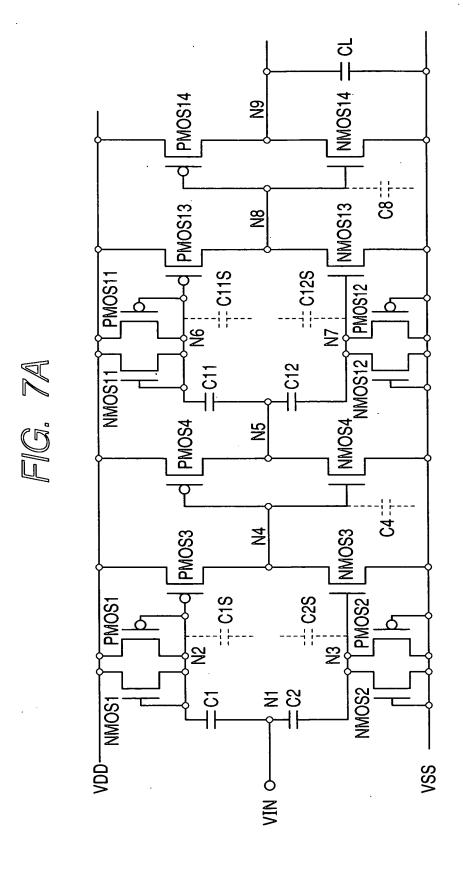
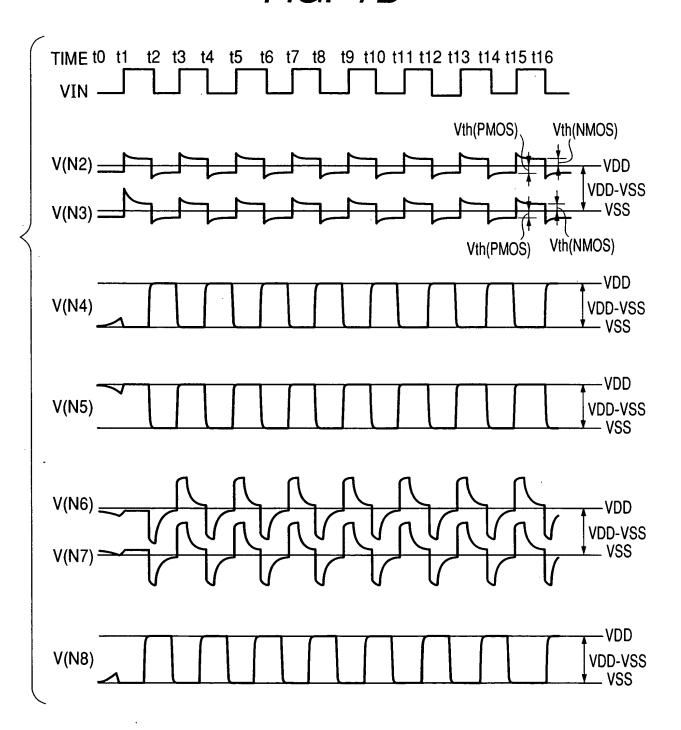


FIG. 7B



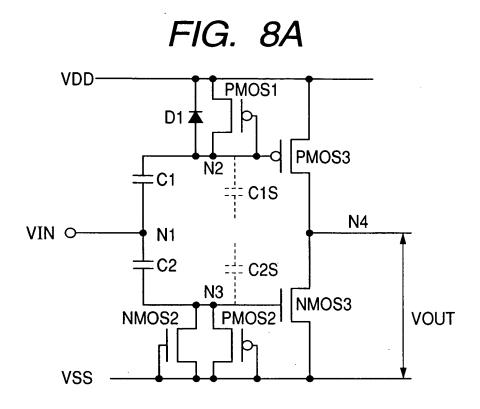


FIG. 8B VDD-NMOS1 PMOS1 PMOS3 N2 C1 === C1S N4 VIN O N1 C2 C2S NMOS3 **VOUT** D2 **Z** VSS

FIG. 8C VDD-PMOS1 D1 本 PMOS3 N2 C1 === C1S **N4** VIN O N1 C2 C2S N3 NMOS3 VOUT D2 **Z** VSS

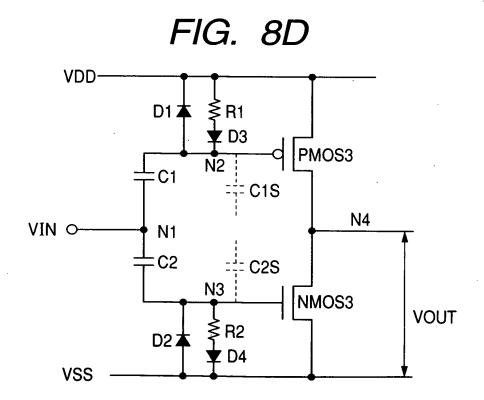


FIG. 9A

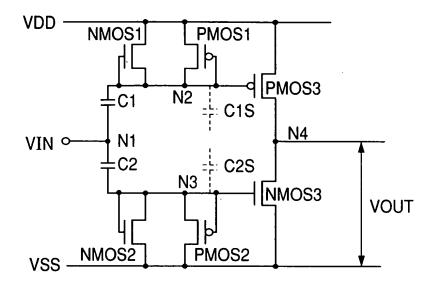


FIG. 9B

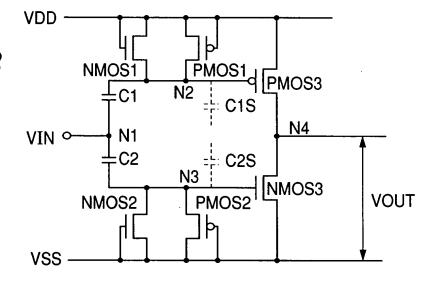


FIG. 9C

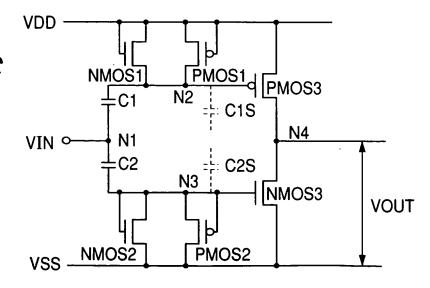


FIG. 10A

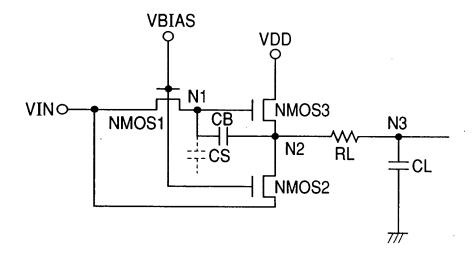
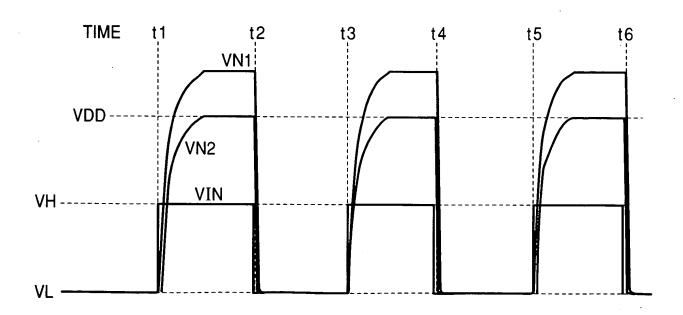


FIG. 10B



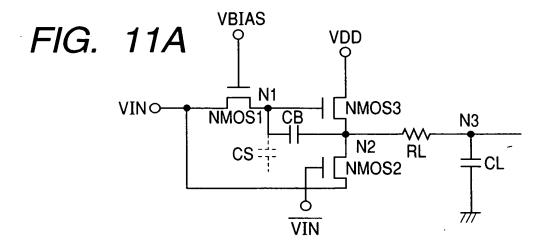
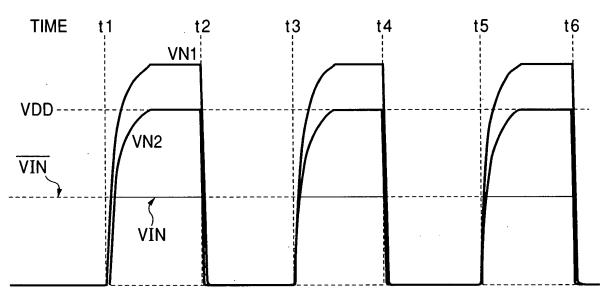


FIG. 11B



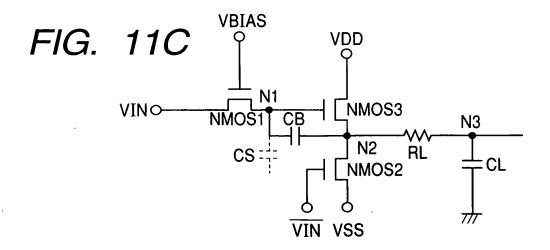


FIG. 12A

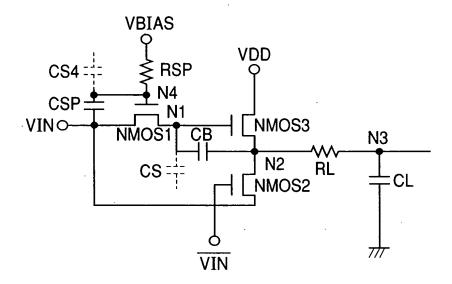


FIG. 12B

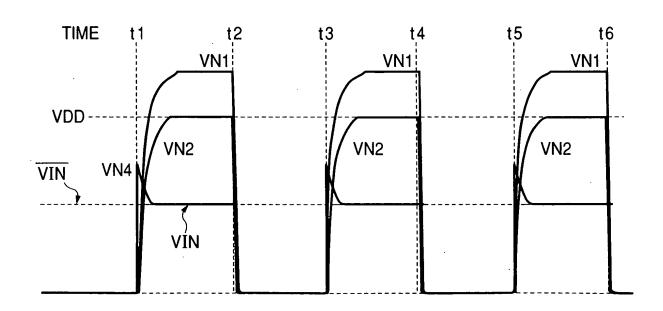


FIG. 13A

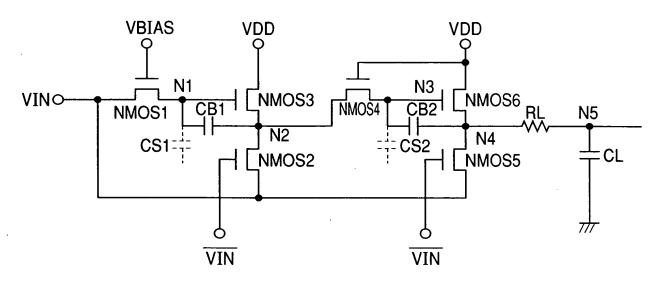
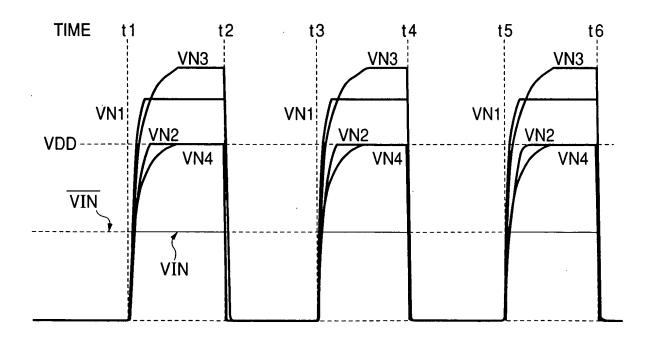


FIG. 13B



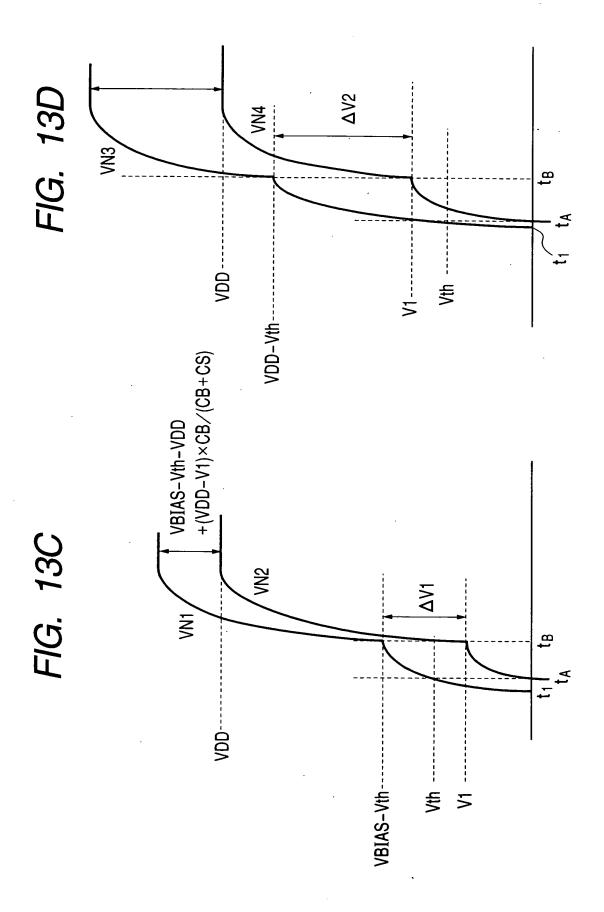


FIG. 14A

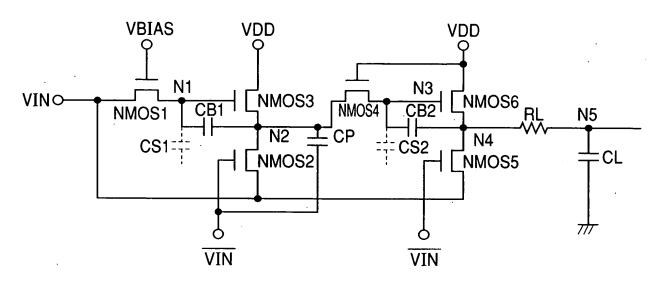
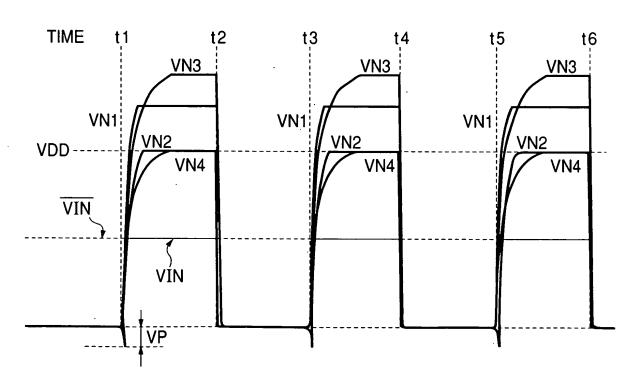


FIG. 14B



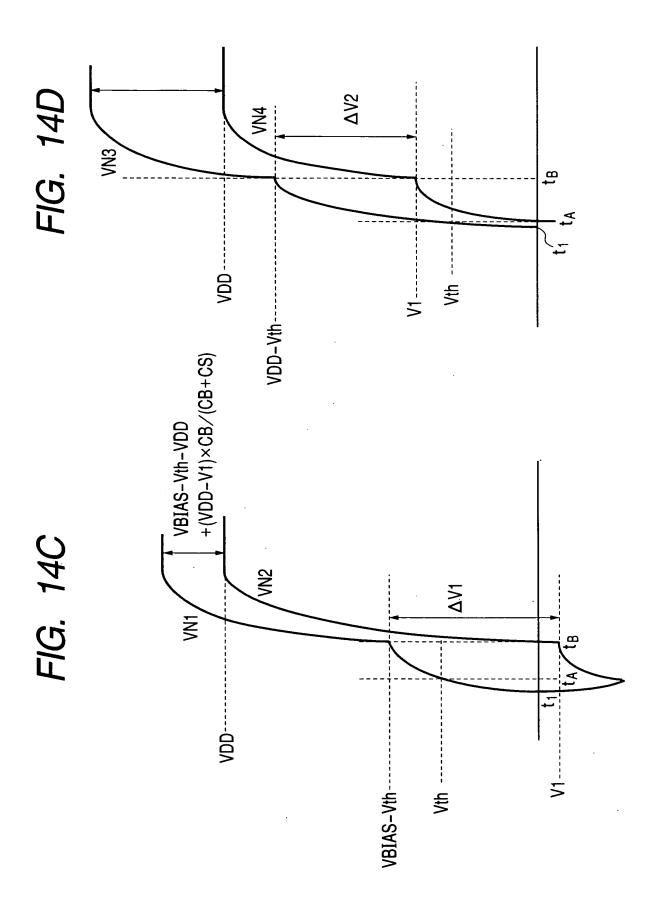


FIG. 15A

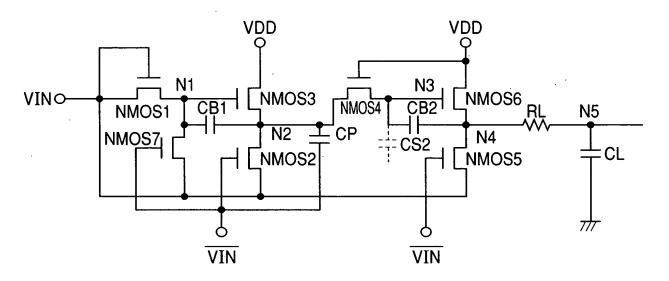
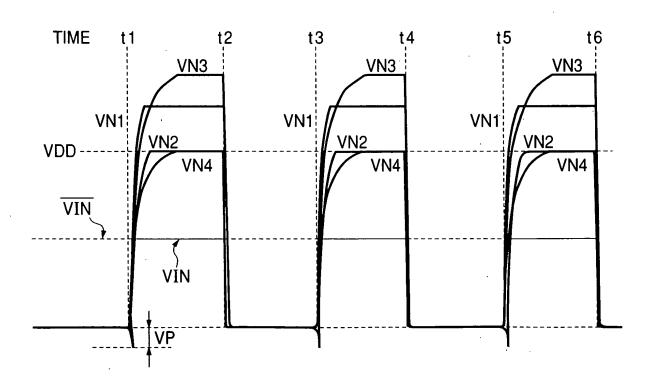


FIG. 15B



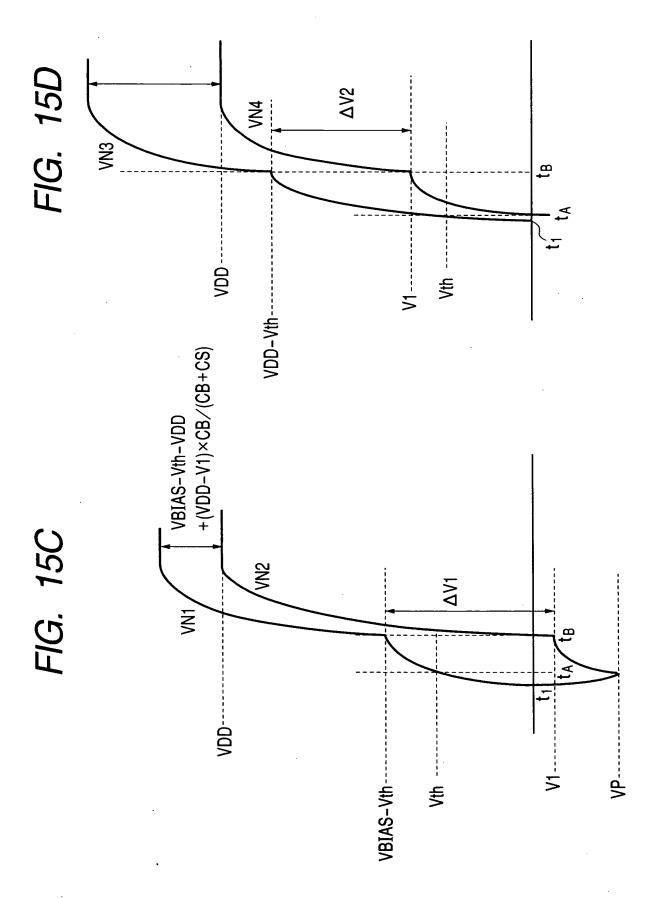


FIG. 16 PRIOR ART

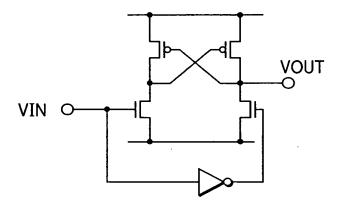


FIG. 17 PRIOR ART

